Hardware Architecture for Realtime Video Coding

30 June, 2021

Koyo Nitta

Agenda

1. Self-introduction
2. Video Coding Technologies
3. MPEG-2 Video Encoder Chips
   - SuperENC,
   - VASA
4. H.264 Video Encoder Chip
   - SARA
5. HEVC Video Encoder Chip
   - NARA
6. Future of Video Coding Chips

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Self-introduction (Basic Information)

- Name: Koyo Nitta (新田 高庸)
- Gender: Man
- Age: 50
- Nationality: Japan
- Residence: Matsunaga

Self-introduction (Occupational History)

- 1995-2001: NTT LSI lab. and NTT Human Interface lab., NTT.
- 2001-2005: Consumer Premises Equipment Division, NTT East.
- 2005-2013: NTT Cyber Space lab., NTT
- 2013-2017: Digital Video Component Business Group, NTT Electronics.
- 2017-2021: Device Innovation Center, NTT.
- 2021-now: The University of Aizu

MPEG-2

H.264

HEVC

NFV/SDN, AI, VVC

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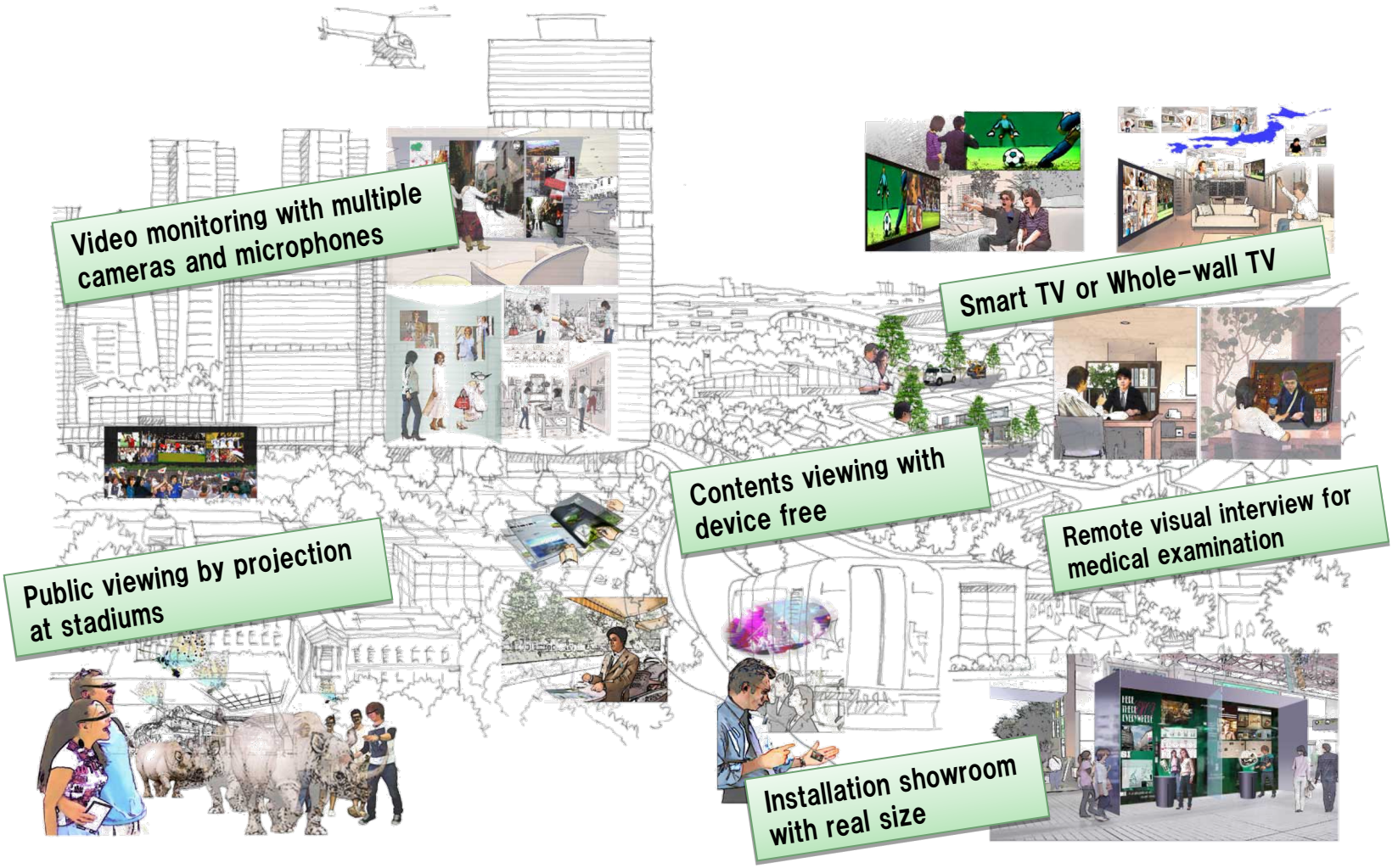
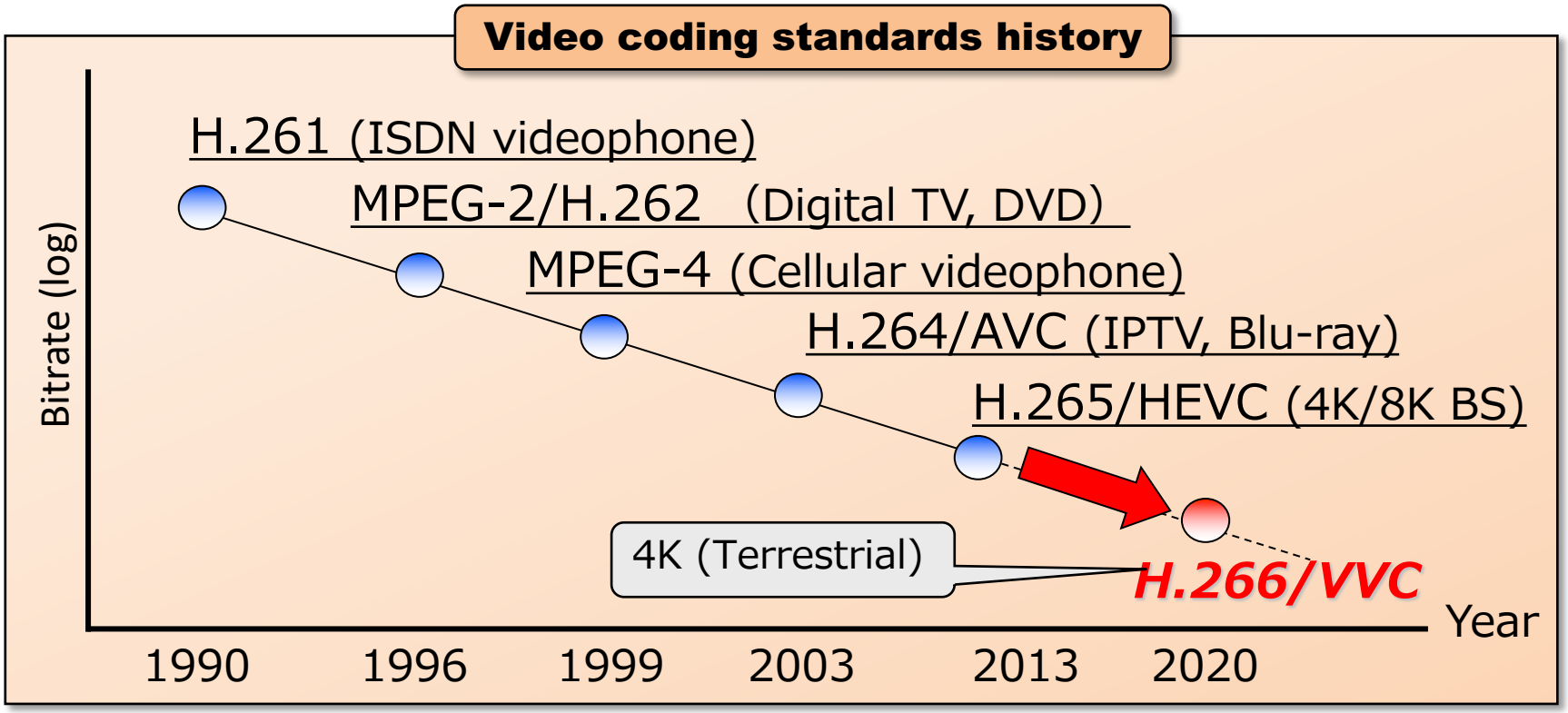
Expansion of Video Coding Applications

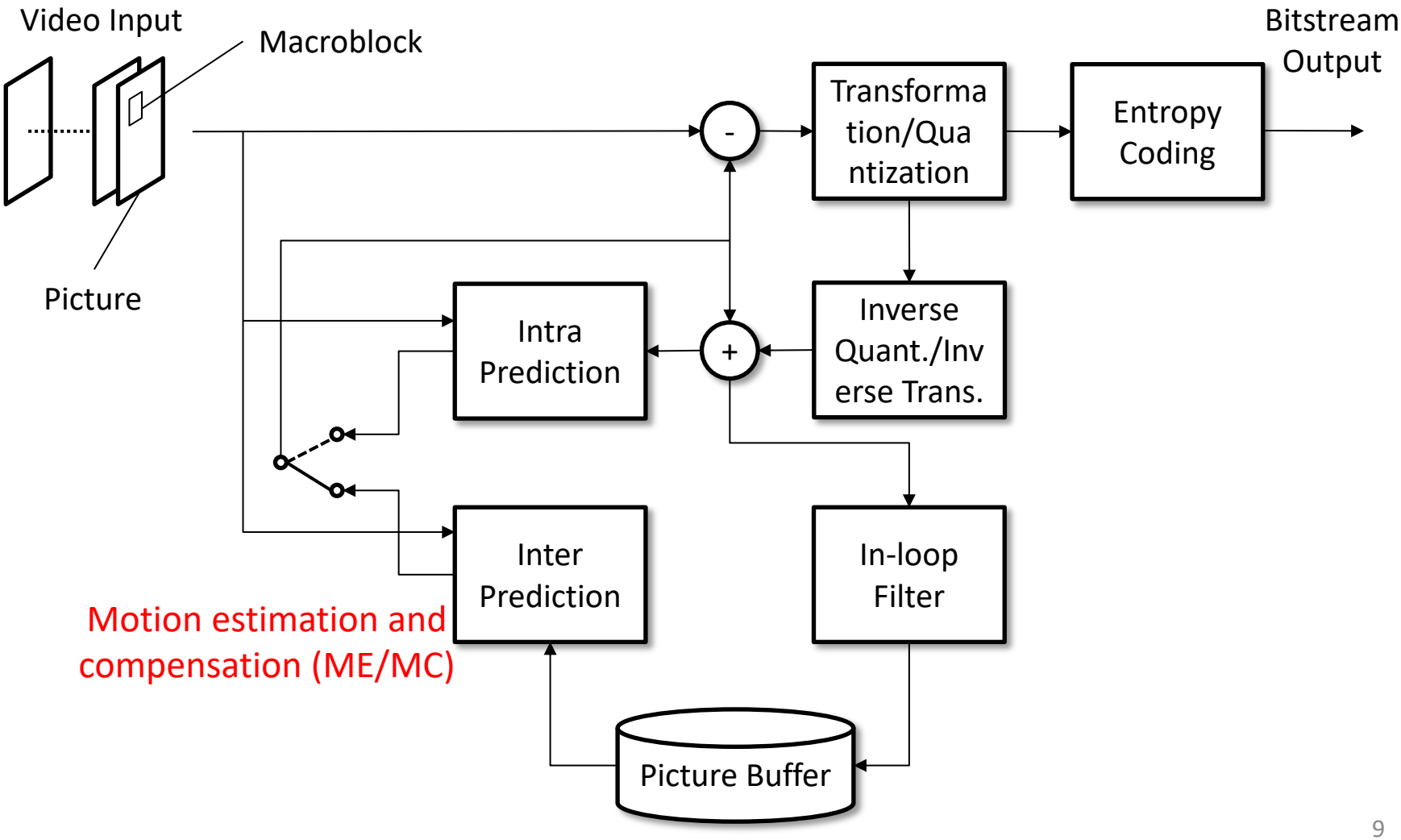


Video Coding Standards

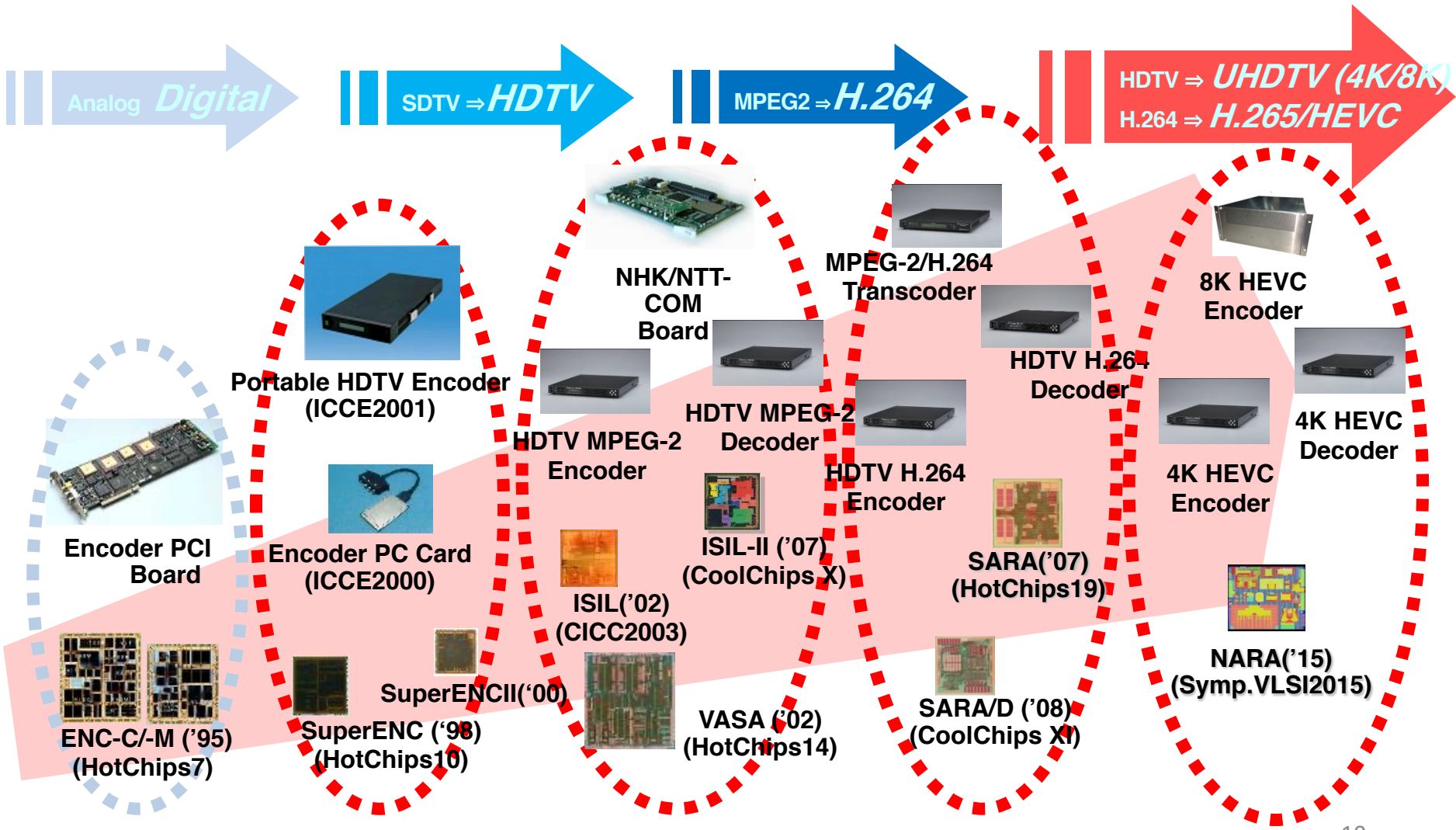
- Video coding standards from ITU (H.26x) and ISO/IEC (MPEG-x).
- Compression ratio tends to be twice per about 10 yrs.



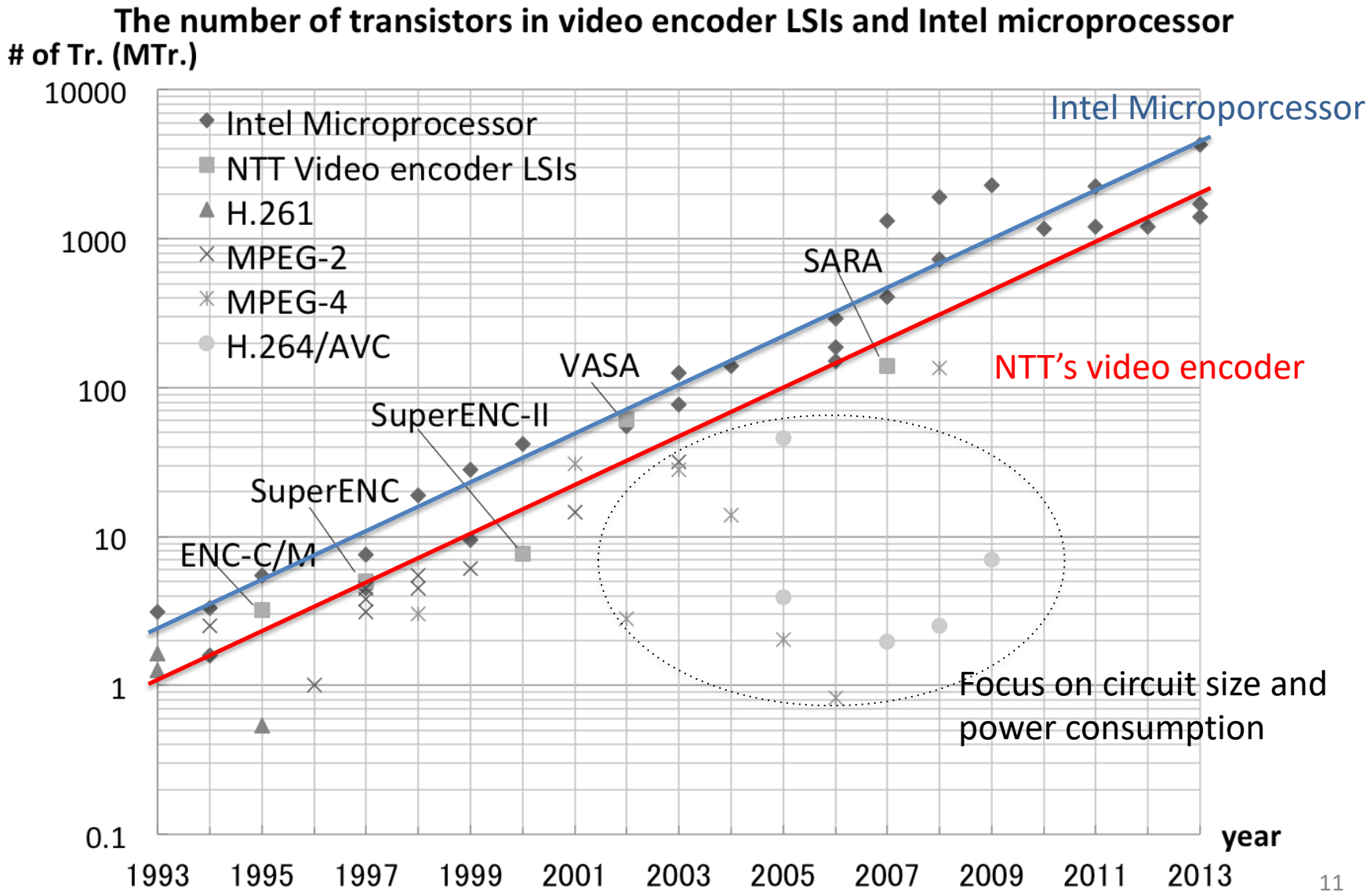
Video coding framework: “MC+DCT”



NTT's Video Codec LSIs and Systems



Video encoder LSIs



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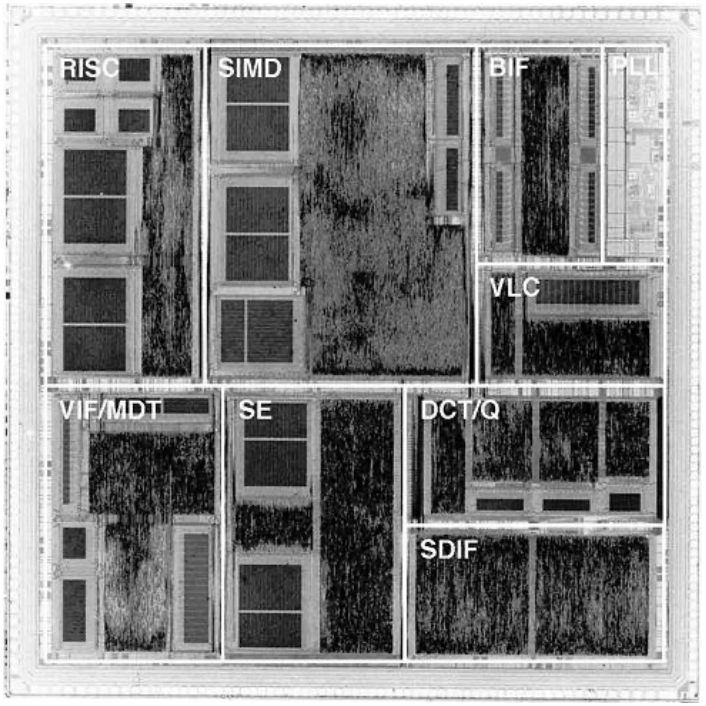
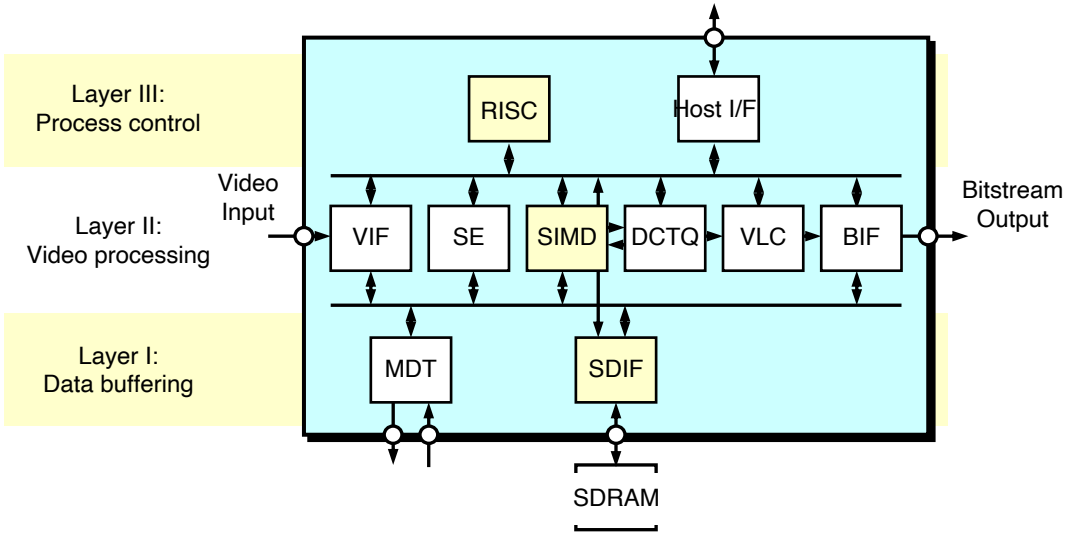
SuperENC – MPEG-2 video encoder LSI

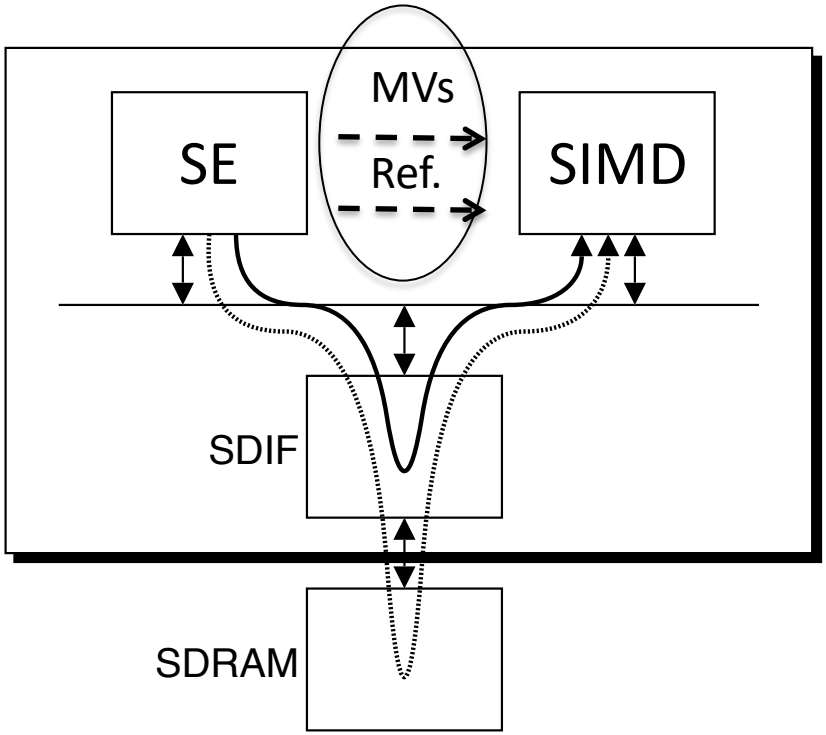
- SIMD processor
- Three-layer Cooperative Architecture / Flexible Communication Architecture





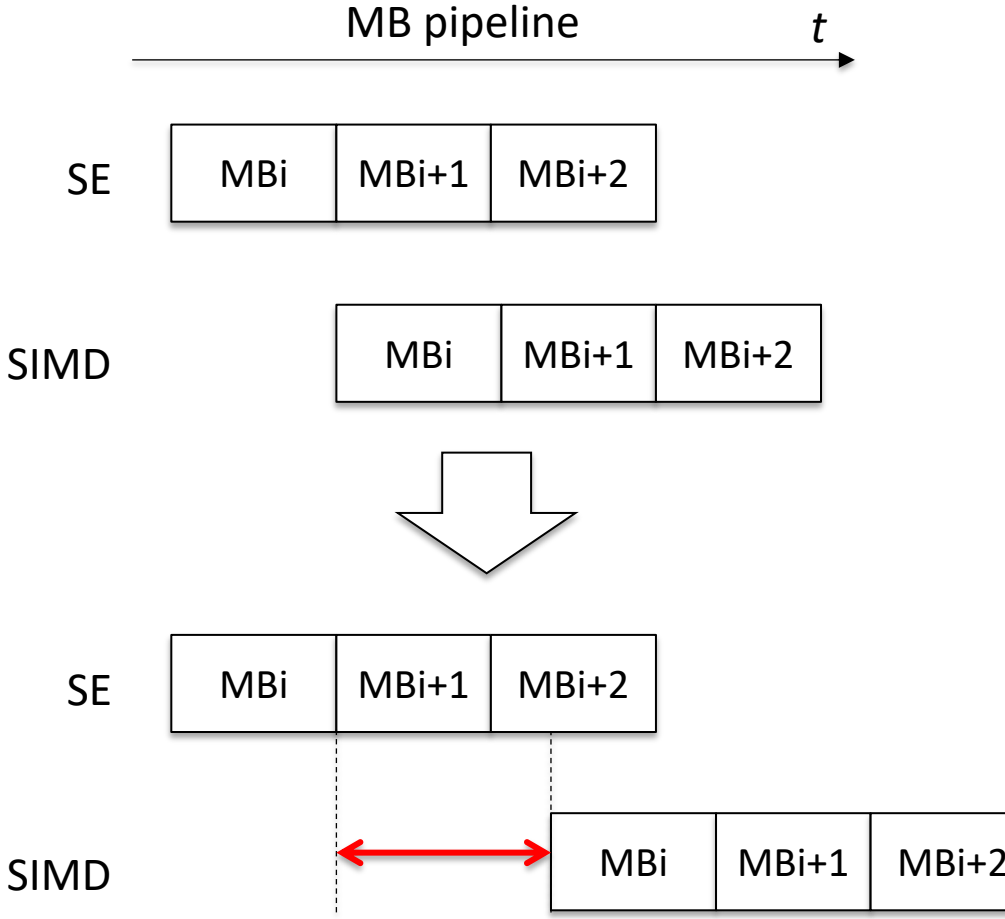
Flexible Communication Architecture

No direct communication



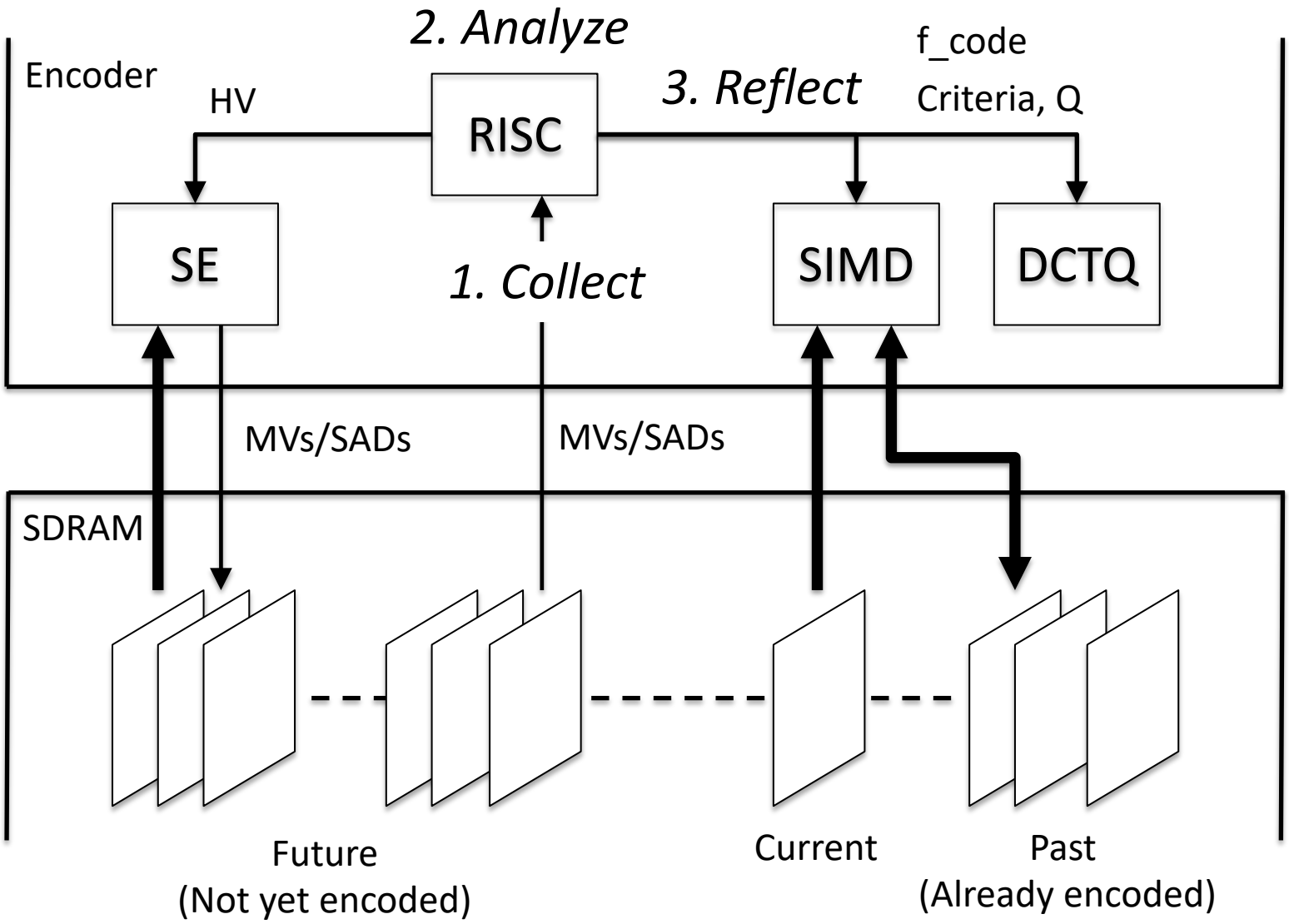
SE: Search Engine (Motion Estimation)

SIMD: SIMD Processor (Motion Compensation)



Any length of time interval can be inserted

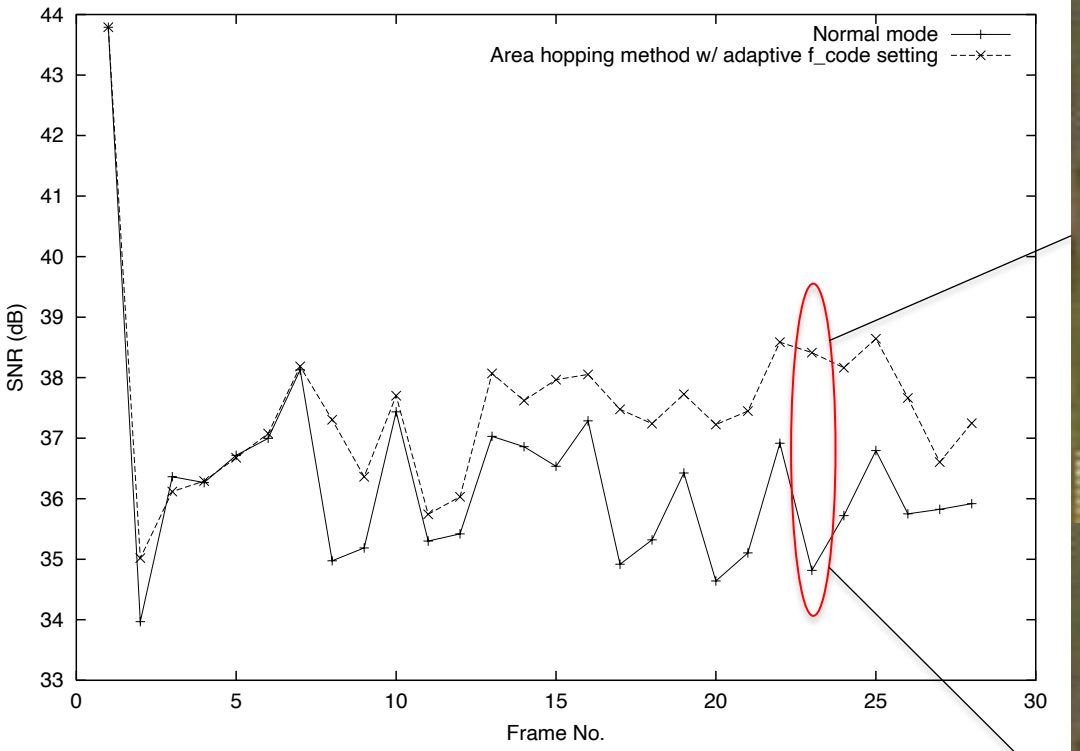
How scene-adaptive algorithm works



Evaluations

Block noise is suppressed

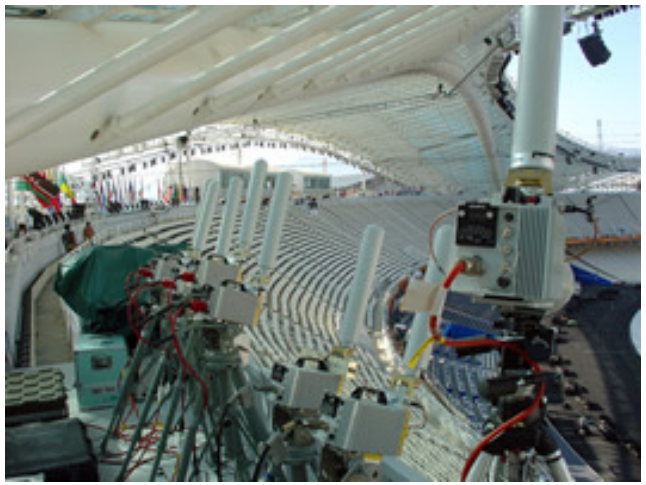
PSNR of “football” sequence.



1.2 dB (average) higher

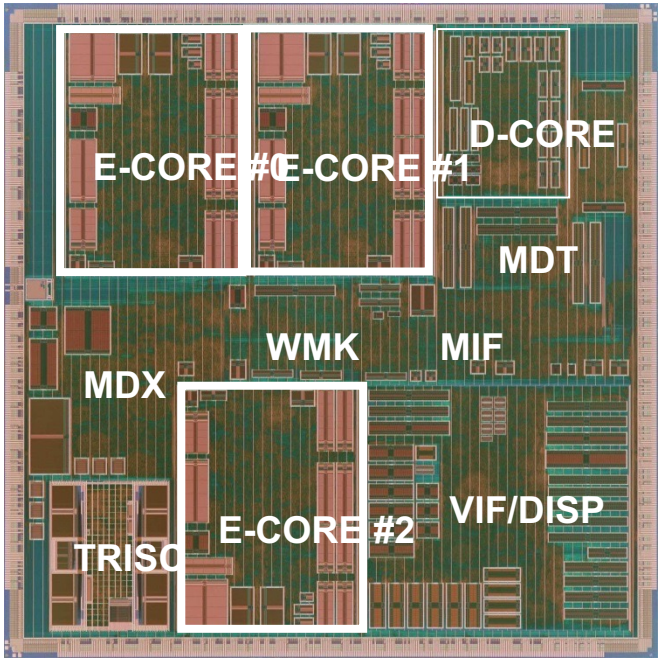
Where SuperENC was used

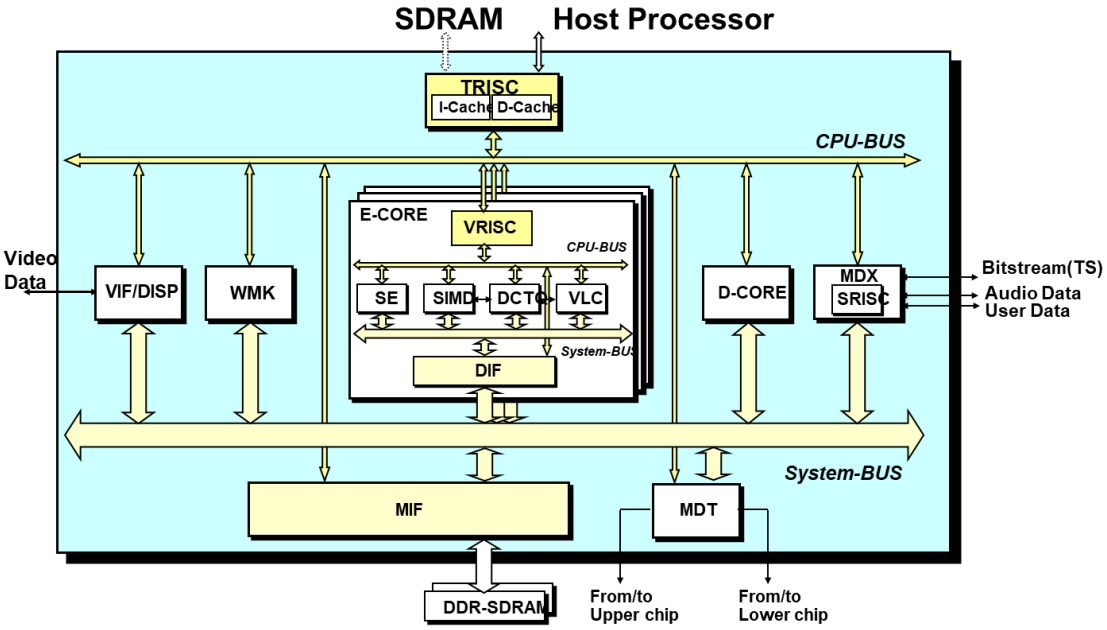
- Athens Olympic games
- America's Cup (Yacht race)
- Golf (Fuji Sankei Classic)
- F-1 (Car race)



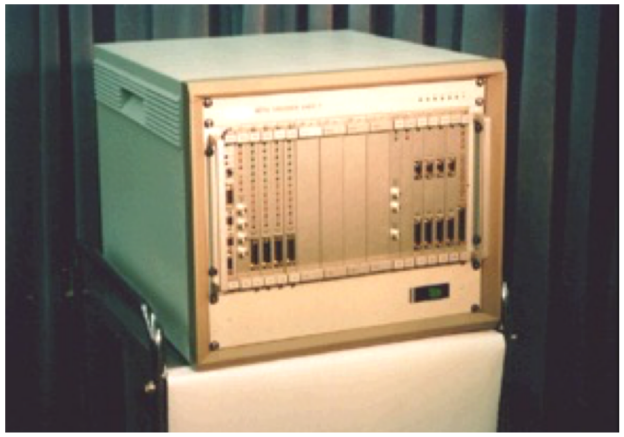
VASA – MPEG-2 HDTV video encoder LSI

- World-first MPEG-2 HDTV encoder LSI
- Multi-core (based on SuperENC)





Downsizing of HDTV encoder system



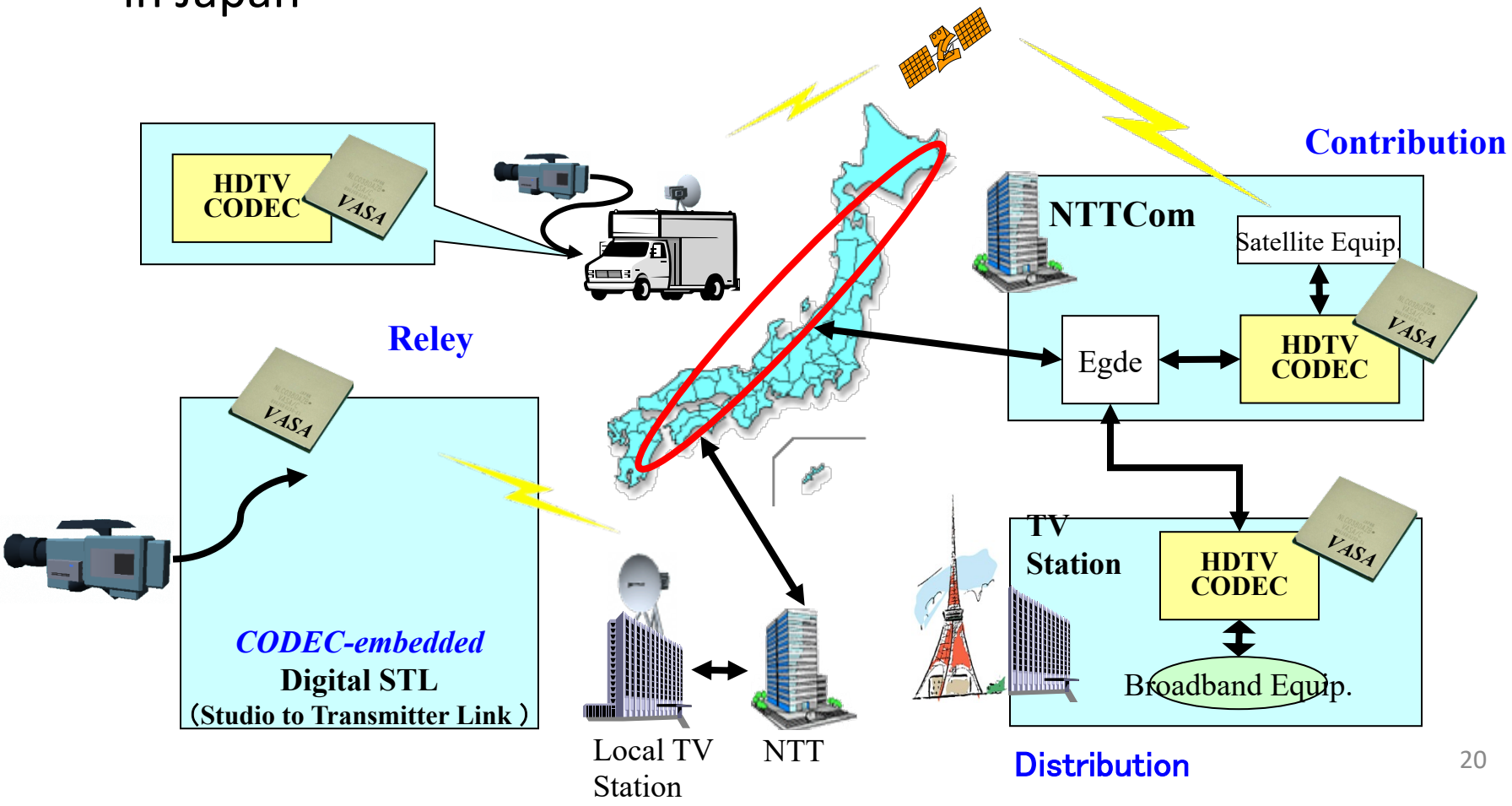
1996: HDTV Encoder (without system LSIs)
10U-full-rack-size / >1000W

2000: Portable HDTV Encoder (with SuperENCx9)
1U-half-rack-size / 80 W

2002: HDTV Encoder (with VASA)
Post-card-size / 15 W
NHK・NTT Com

Digital TV broadcasting network

- HDTV transmission network for digital terrestrial broadcasting in Japan



Where VASA and HDTV systems were used

Shinjuku BS-I Stadio (2000.12-2002)

FIFA World Cup (2002.6)

NHK Guilin live (2003.9)

NHK Antarctic Live (2003.11)

NHK Athens Olympic (2004.8)

US President election (2004.11)

NHK Aurora Live (2003.9)

- **NHK**
- **Korea MBC**
- **UK BT**

Turin Olympic (2006.2)

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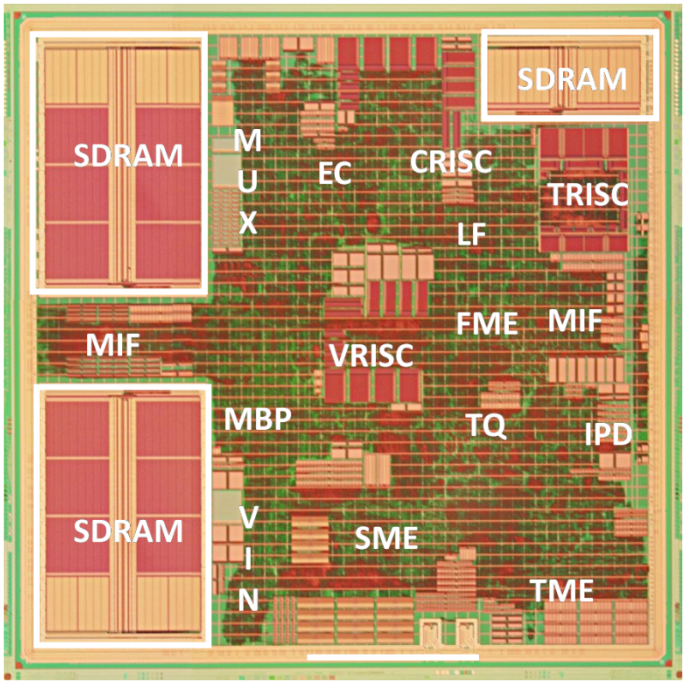
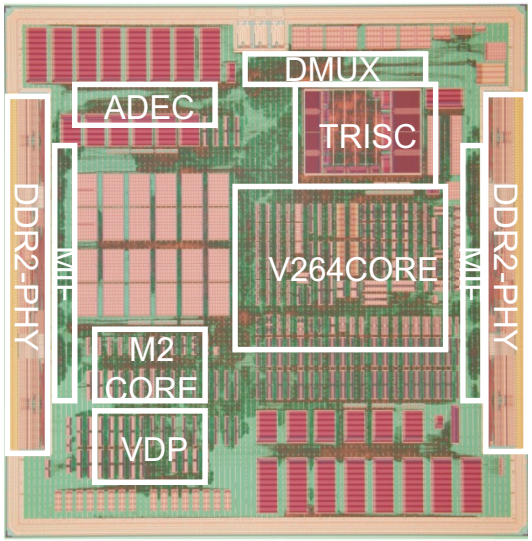
SARA – H.264 video CODEC LSIs

- IP retransmission service
- Embedded DRAM (SARA/E)



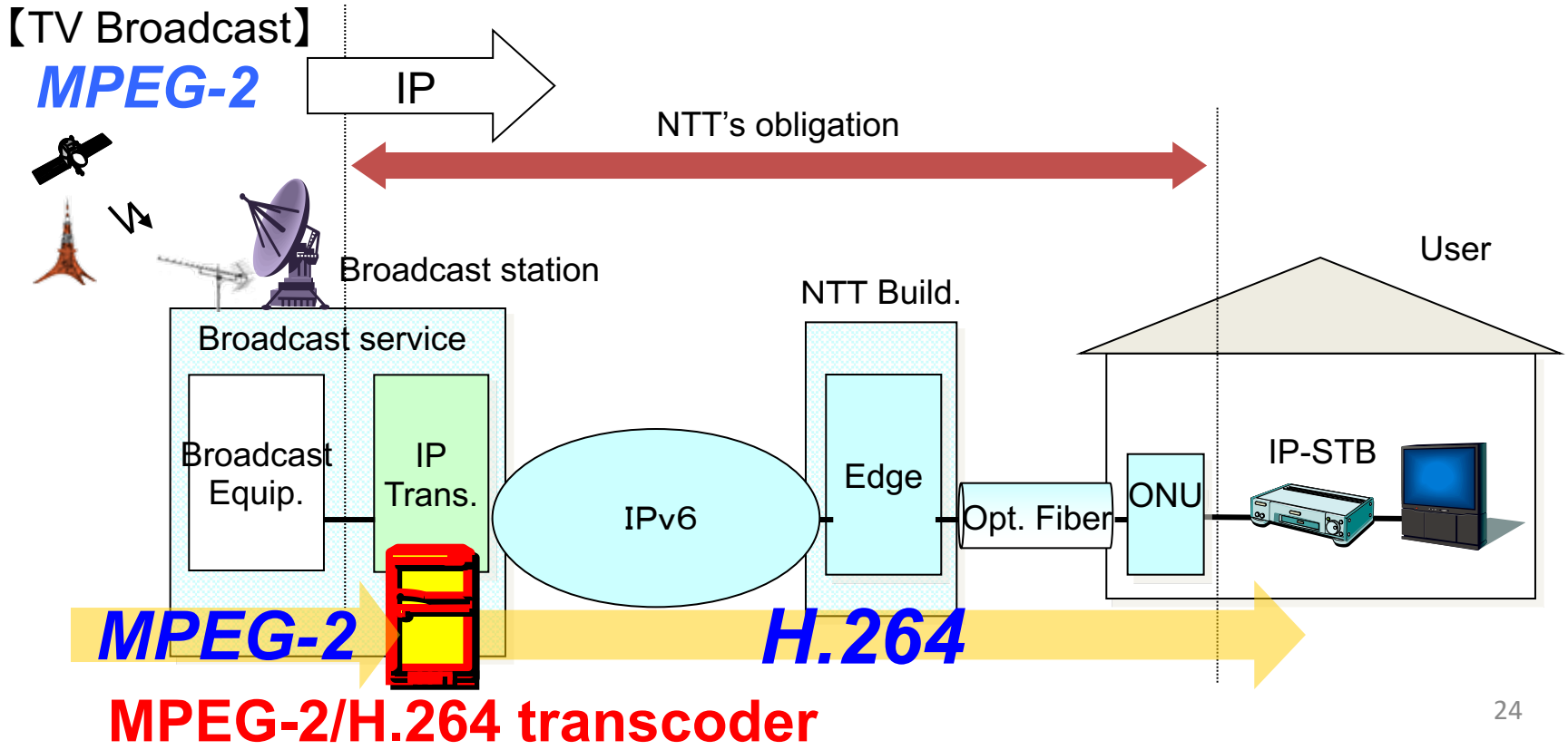
SARA/E (Encoder)



SARA/D (Decoder)

IP retransmission service

- For rural area where it is hard to receive digital terrestrial TV service.
- Thanks to H.264, IP bandwidth can be reduced.



Where SARA was used

Sochi Olympic (2014)

London Olympic (2012)

FIFA World Cup (2010)

MLB.NW / MLB.COM (2009)

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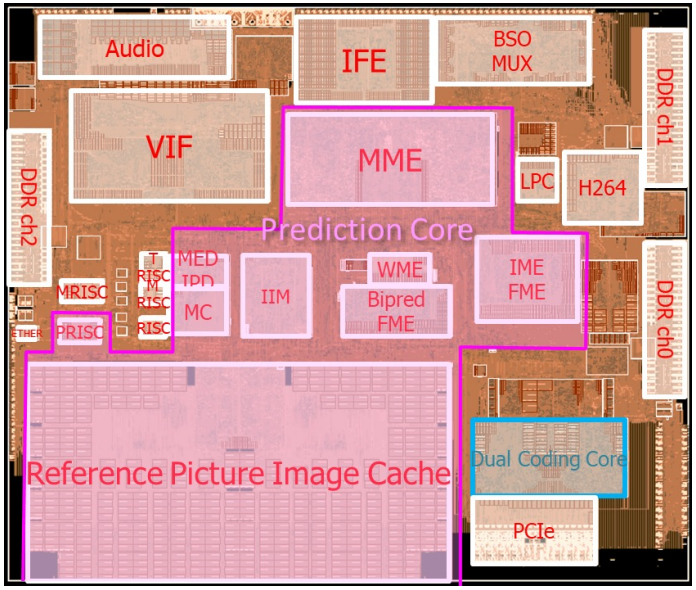
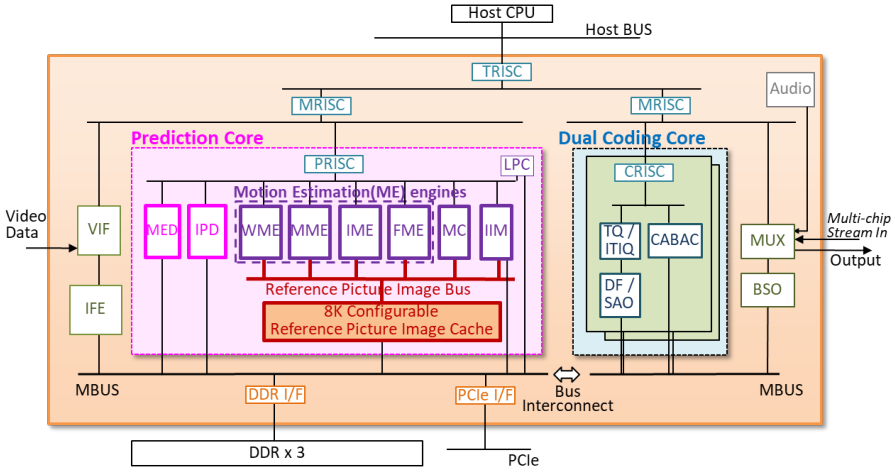
NARA – HEVC 4K encoder LSI

- Heterogeneous parallelism
- MIC project (w/ Fujitsu)





Where NARA is used

- 4K/8K TV broadcasting services (2018-)

8K HEVC encoder

4K/8K Broadcasting

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NTT video encoder chips: Pros and Cons

- Pros:
  - High quality of image
    - Acceptable for professional use
  - Very low latency
    - < 100ms delay can be achieved.
- Cons:
  - Larger circuit area
    - Higher power consumption
    - Higher cost
    - Longer development time

How to reduce circuit area
without sacrifying quality of image

Real time processing approach

- General Purpose Processor (CPU, GPU) and AI accelarator
  - Faster is better,
  - But, no explicit timing constraints
- Real time processor (like video codec)
  - Any input data must be processed in real time.
    - Therefore, memory cache in CPU cannot be used.
  - Macroblock pipeline is usually used.

Any other cache or parallelism ?

without violating realtime constraints

Conclusions

- Several Video Encoder Chips were developed
  - MPEG-2 (SuperENC, VASA),
  - H.264 (SARA),
  - HEVC (NARA)
- They are mainly used for broadcasting services.

- VVC has standardized.
  - What kind of VVC encoder chips are required?
    - Hardware algorithm
    - New realtime processing architecture

Thank you for listening